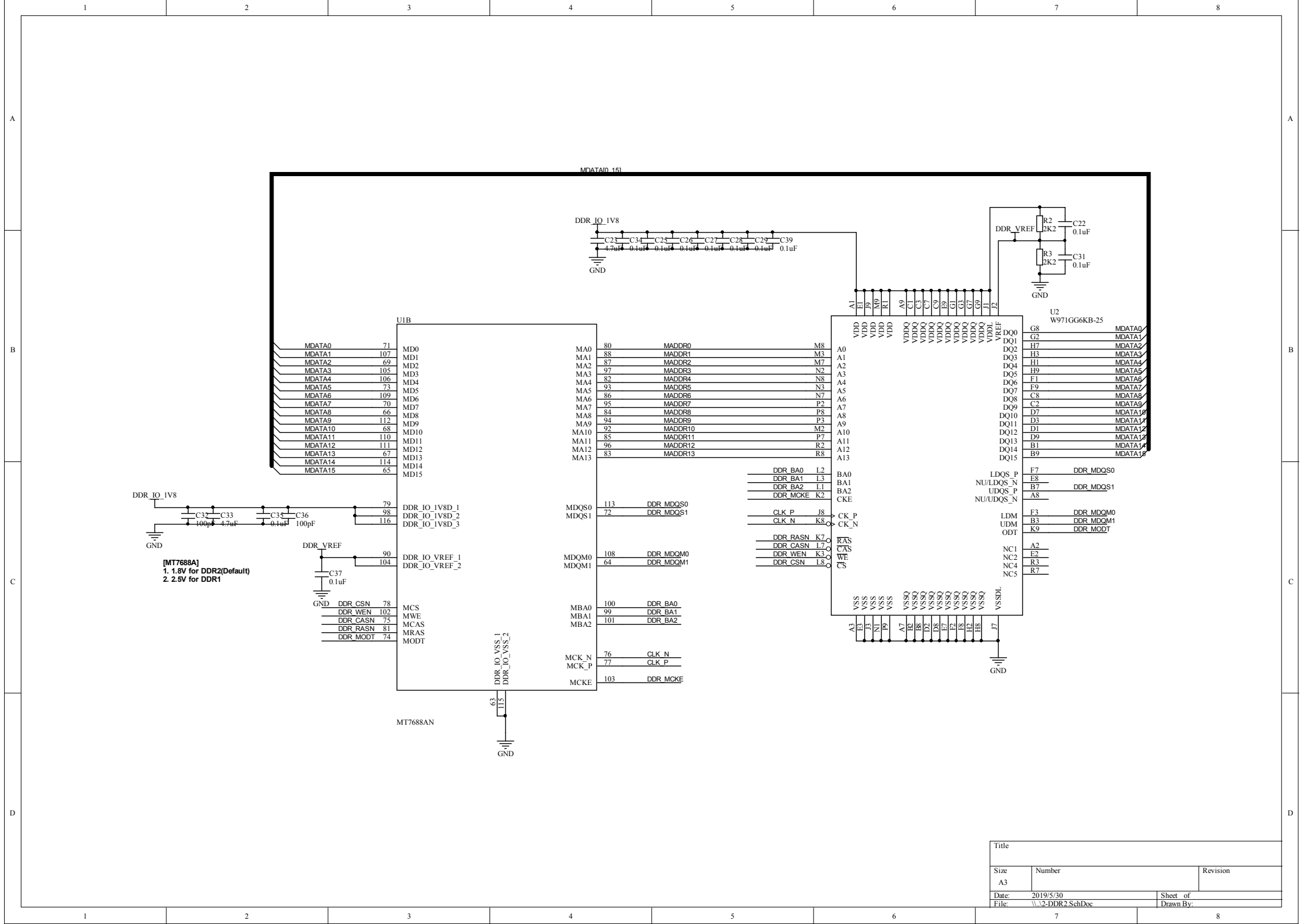


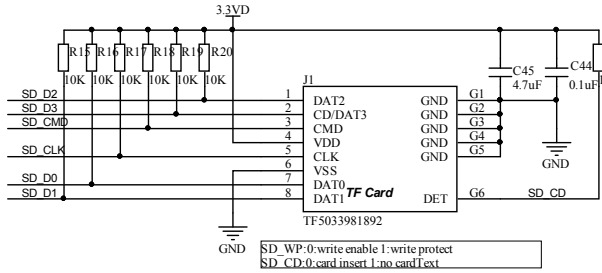
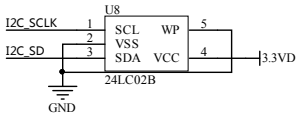
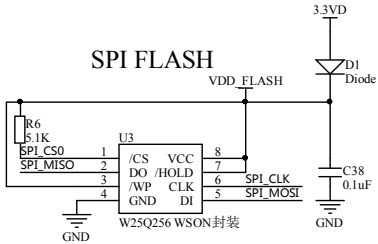
PIN	7688	7628
9	NC	GND
12	NC	WF1_P
11	NC	WF1_N

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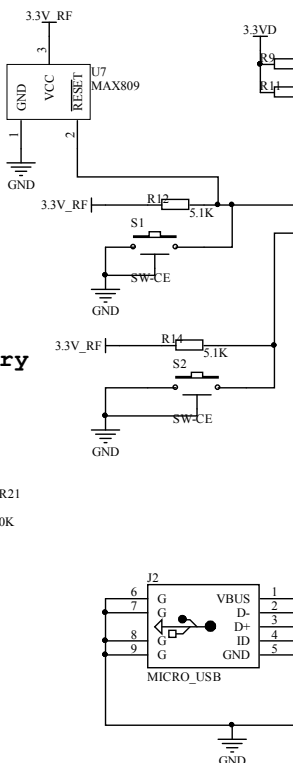
SPI FLASH



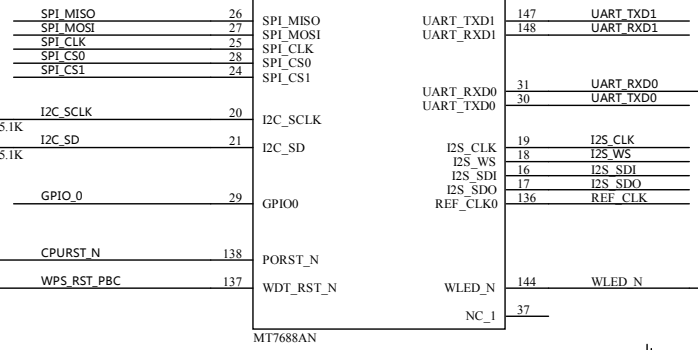
SD_WP:0:write enable 1:write protect
SD_CD:0:card insert 1:no cardText

Reset

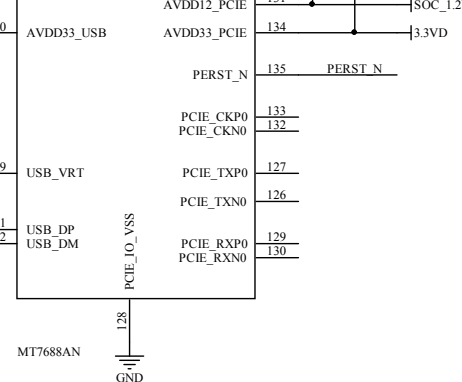
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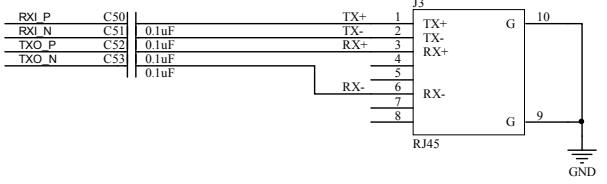
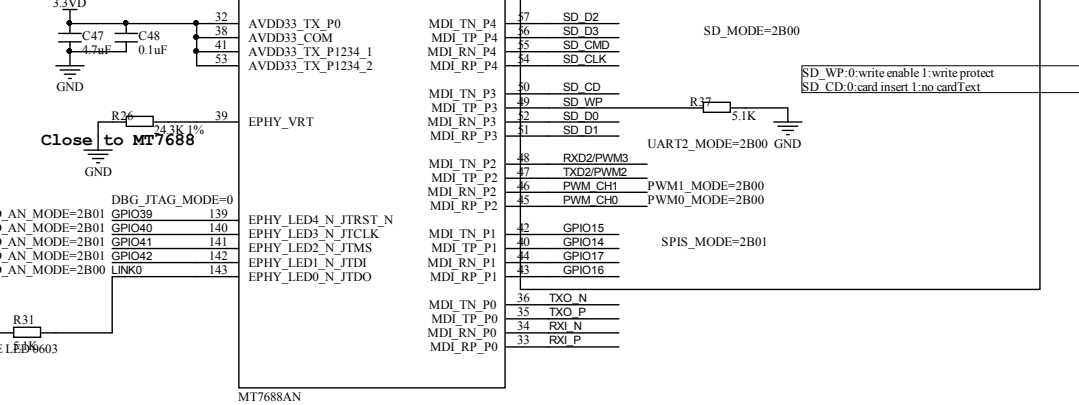
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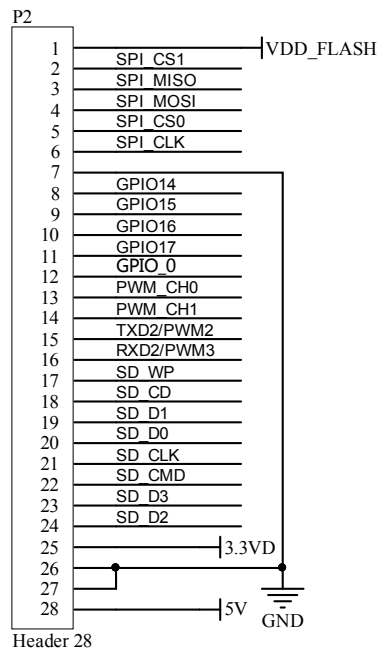
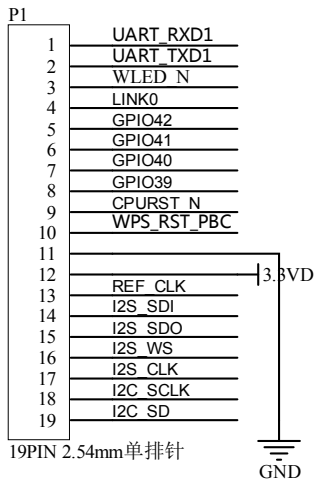
UID



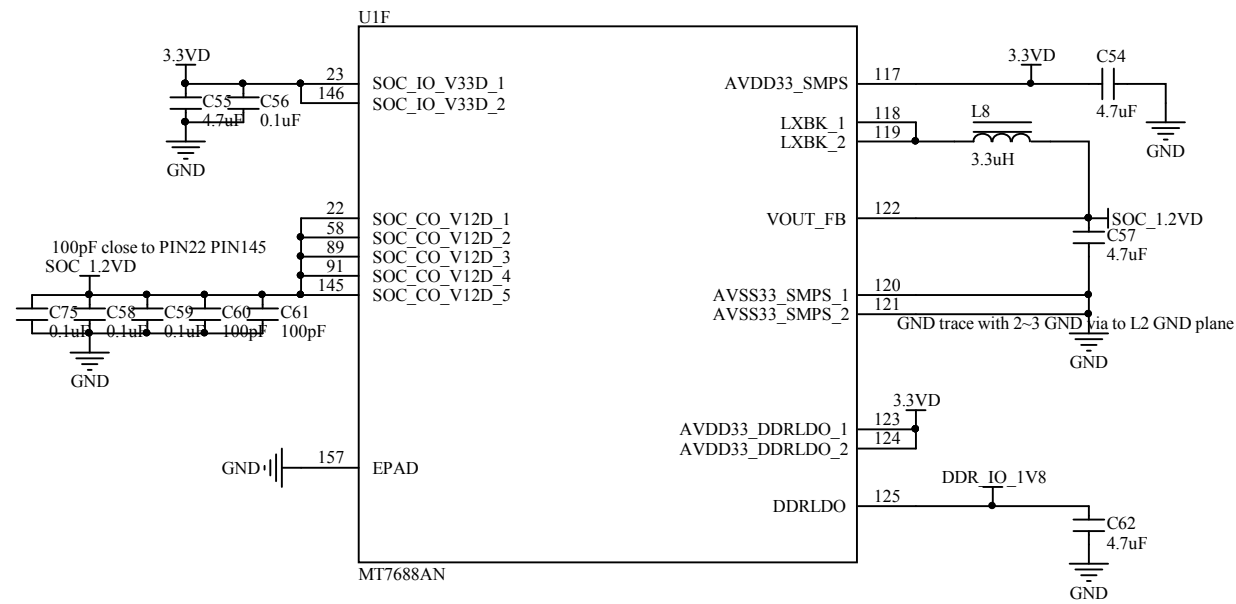
UIE



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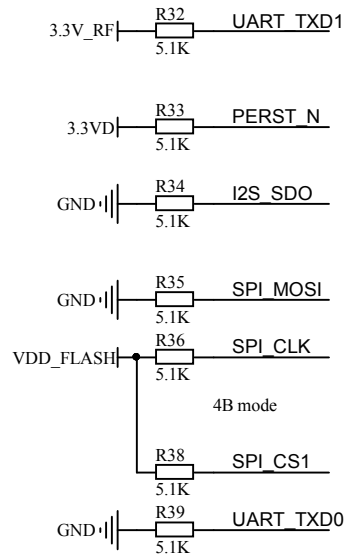


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[MT7688AN-IOT] 1. 1.8V for DDR2 2. 2.5V for DDR1 configured by SW

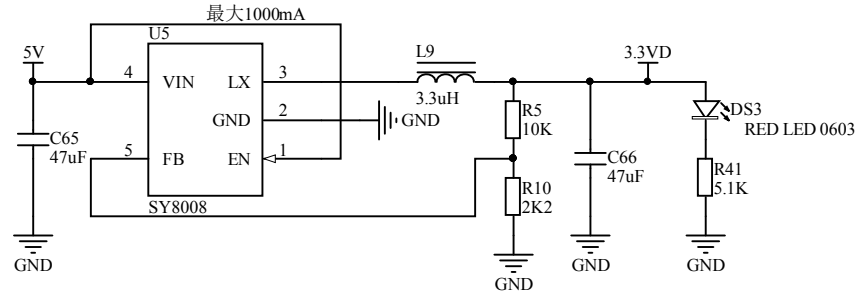
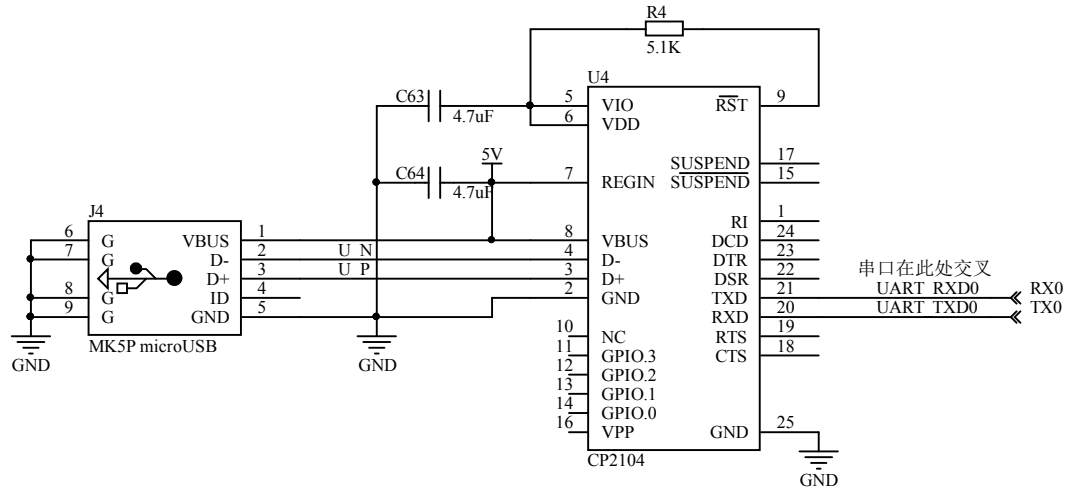
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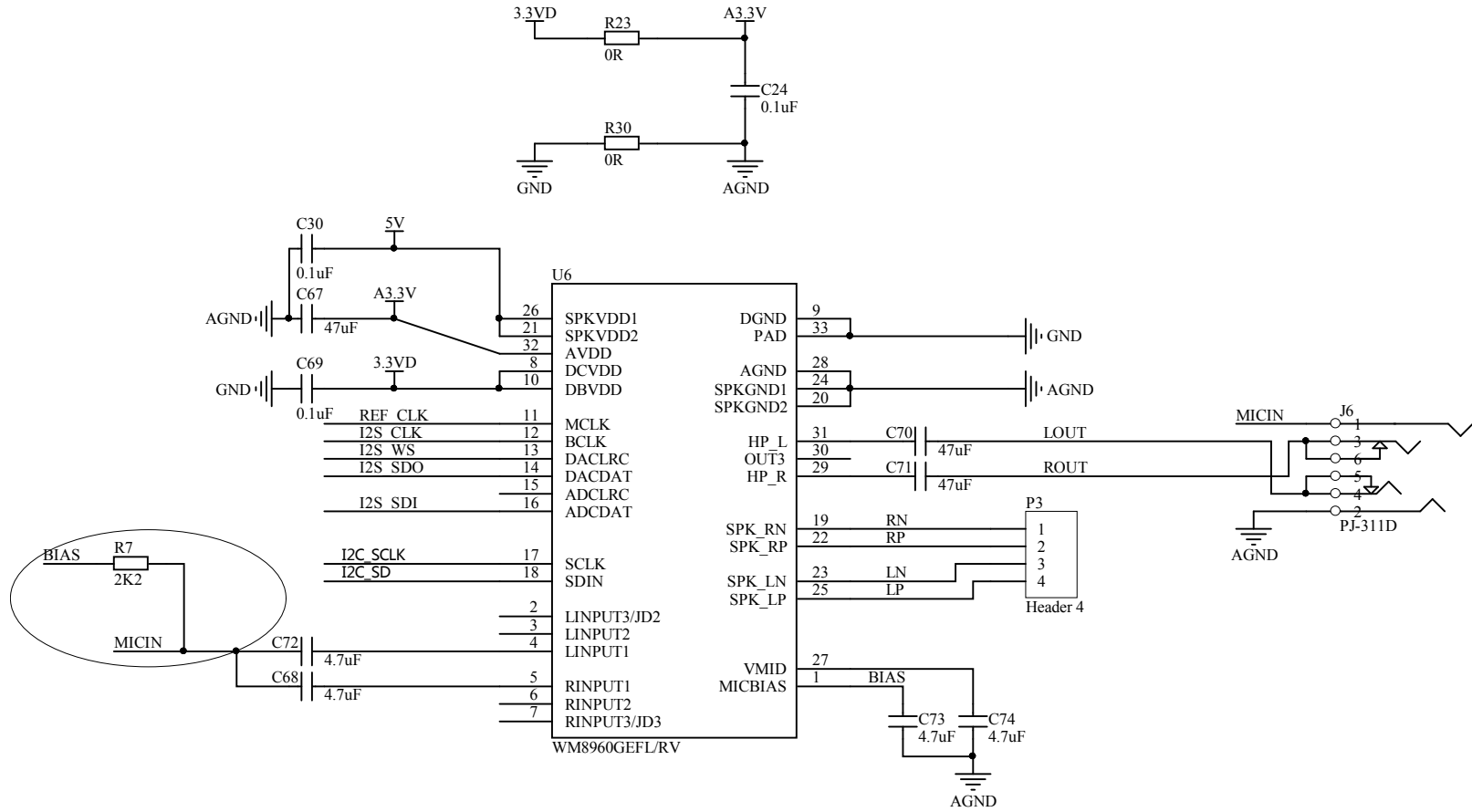
Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
{SPI_MOSI SPI_CLK, SPI_CS1}	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

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Title		
Size A4	Number	Revision
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File:	\\.\8-AUDIO.SchDoc	Drawn By: